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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/775,230	02/01/2001	Hoi-Jin Lee	SAM-0192	9045

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EXAMINER	
O'BRIEN, BARRY J	

ART UNIT	PAPER NUMBER
2183	7

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DATE MAILED: 12/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/775,230	LEE, HOI-JIN	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/01/01, 4/02/01 and 12/04/01*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-11 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Priority Documents as received on 2/01/2001, Declaration as received on 4/02/2001 and Power of Attorney as received on 12/04/2001.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The abstract is objected to for containing the purported merits of the invention on lines 10-14. Please see below.

5. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Claim Objections

6. Claims 4 and 8 are objected to because of the following informalities:

   a. Regarding claim 4, please correct the language "performing an exclusive-OR operation to the process ID" to correctly read –performing an exclusive-OR operation on the process ID" to eliminate confusion as to what the inputs of the exclusive-OR are.

   b. Regarding claim 8, please correct the language "counts decrements" to correctly read --the counter decrements-- to align with the language in the rest of the claim.

7. Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 8-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claim 8 recites the limitation "counter" in its first line. There is insufficient antecedent basis for this limitation in the claim. For the purposes of this examination, it will be assumed that the "counter" in question refers to the "up/down saturating counters" as claimed in claim 2. Please correct the claim language and/or claim dependencies to correct this lack of antecedent problem.

11. Claim 9 recites the limitation "shift register" in its first line. There is insufficient antecedent basis for this limitation in the claim. For the purposes of this examination, it will be assumed that the "shift register" in question refers to the "history register" which comprise a shift register as claimed in claim 3. Please correct the claim language and/or claim dependencies to correct this lack of antecedent problem.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Talcott, U.S. Patent No. 6,272,623.

14. Regarding claim 1, Talcott has taught a branch predictor for a multi-processing computer comprising:

a. A history register (240 of Fig.2) for storing a branch history of previous sequential branch instructions (see Col.3 lines 44-52),

b. A hash logic (250 of Fig.2) for creating an index from a combination of process references corresponding to a current branch instruction, an address of the current branch instruction, and the branch history (see Col.3 lines 6-9, 56-59),

c. A branch prediction table (260 of Fig.2) for storing branch prediction reference data, and for outputting branch prediction reference data corresponding to the index created by the hash logic (see Col.3 line 60 to Col.4 line 7),

d. An address selection circuit for selecting one of a target address known from the current branch instruction and a next instruction of the current branch instruction to generate a branch prediction address, in response to the branch prediction reference data output from the branch prediction table. While not shown explicitly, it is inherent that the IFU (290 of Fig.2), upon receiving the branch prediction, will select between a branch target address and an instruction following the branch instruction based on the prediction outputted of branch prediction system (200 of Fig.2) because action is taken on the branch prediction in the IF stage rather than in the branch prediction system (see Col.2 lines 1-10 and Col.5 lines 14-20). Furthermore, if there was no instruction selected based on a branch prediction, then having branch prediction in the processor would be moot and an extraneous feature, adding unnecessary hardware and complexity to the system.

e. A branch prediction result tester for updating the branch history stored in the history register and the branch prediction reference data stored in the branch prediction table, in response to a real branch address and the branch prediction address according to an execution result of the current branch instruction. Here, because branch prediction is based on the fact that future outcomes of conditional branches will be similar to prior outcomes (see Col.2 lines 1-10), and because Talcott has taught the storing the results of prior branch instructions in the history register and the branch prediction table (see Col.3 lines 35-41, 47-50), it is inherent that a branch instruction has been executed and the results of the execution are used to update the history register and branch prediction table.

15. Regarding claim 2, Talcott has taught the branch predictor of claim 1, wherein the branch prediction table comprises a plurality of up/down saturating counters selected by the index created by the hash logic (see Col.3 line 60 to Col.4 line 7).

16. Regarding claim 3, Talcott has taught the branch predictor of claim 1, wherein the history register comprises a shift register (see Col.3 lines 44-52).

17. Regarding claim 4, Talcott has taught the branch predictor of claim 1, wherein the hash logic creates the index by performing an exclusive-OR operation to the process ID corresponding to the current branch instruction (see Col.3 lines 31-43), the address of the current branch instruction, and the branch history (see Fig.2 and Col.3 lines 6-9, 56-59). Here, the local history table (220 of Fig.2) comprises results of a set of instructions with some address bits in common (see Col.3 lines 31-43), which corresponds to the locality that a process uses when executing. Thus these address bits, which correspond to a group of "local" instructions, are considered a

process ID because they identify a process, and each process, and its corresponding instructions, will have a different location in memory, and thus a different set of address bits in common.

18. Regarding claim 5, Talcott has taught the branch predictor of claim 1, wherein the branch prediction result tester includes a comparator for determining whether a real branch address according to an execution result of the current branch instruction matches with the branch prediction address, and creating a control signal corresponding to the result (see Col.3 lines 35-41, 47-50). Here, as shown above in paragraph 12, it is inherent that a branch instruction has been executed and the results of the execution are used to update the history register and branch prediction table. The register and table must be updated to contain accurate information so that branches can be predicted accurately and in an educated manner (see Col.2 lines 1-10). In order to determine if a prediction was correct, one has to compare what was predicted to what the actual outcome was. If the predicted outcome matches the actual outcome, the prediction was correct. If the predicted outcome differs from the actual outcome, the prediction was incorrect.

19. Regarding claim 6, Talcott has taught the branch predictor of claim 5, wherein the comparator generates a control signal of logic "1" if the real branch address matches with the branch prediction address, and generates a control signal of logic "0" if the real branch address does not match (see Col.3 lines 45-51, Col.3 line 60 to Col.4 line 7). Here, a logic value of "1" corresponds to a taken branch, and a logic value of "0" corresponds to a not taken branch.

20. Regarding claim 7, Talcott has taught the branch predictor of claim 6, wherein the address selection circuit changes and outputs the real branch address to the corrected branch address when the control signal is logic "0" (see Col.3 lines 44-50, Col.3 line 60 to Col.4 line 7). Here, when the control signal is "0", a branch has been predicted incorrectly (see above

paragraph 17). Therefore it is inherent that the real, correct branch address be selected and subsequently output to the instruction fetch circuitry (290 of Fig.2) so that the microprocessor operates correctly.

21. Regarding claim 8, Talcott has taught the branch predictor of claim 6, wherein the counter increments when the control signal is logic "1", and counts decrements when the control signal is logic "0" (see Col.3 line 60 to Col.4 line 7).

22. Regarding claim 9, Talcott has taught the branch predictor of claim 6, wherein the shift register shifts the branch prediction result in a first direction by inserting the control signal (see Col.3 lines 44-50). Here, a "1" is shifted into the shift register when a branch is taken, which corresponds to the control signal being "1", and a "0" is shifted in when the branch is not taken, which corresponds to the control signal being "0", as described above in paragraph 17.

23. Regarding claim 10, Talcott has taught a prediction method of a branch address of a conditional branch instruction with reference to a branch prediction table for storing branch prediction reference data, the method comprising the steps of:

a. Creating an index to access the branch prediction table from a combination of a process ID corresponding to the conditional branch instruction, an address of the conditional branch instruction, and previous sequential branch instructions (see Fig.2 and Col.3 lines 6-9, 56-59). Here, the local history table (220 of Fig.2) comprises results of a set of instructions with some address bits in common (see Col.3 lines 31-43), which corresponds to the locality that a process uses when executing. Thus these address bits, which correspond to a group of "local" instructions, are considered a process ID because they identify a process, and each

process, and its corresponding instructions, will have a different location in memory, and thus a different set of address bits in common.

b. Reading branch prediction reference data from the branch prediction table in response to the index (see Col.3 line 60 to Col.4 line 7).

c. Selectively outputting one of a target address known from the conditional branch instruction and a next address of the conditional branch instruction in response to the branch prediction reference data. While not shown explicitly, it is inherent that the IFU (290 of Fig.2), upon receiving the branch prediction, will select between a branch target address and an instruction following the branch instruction based on the prediction outputted of branch prediction system (200 of Fig.2) because action is taken on the branch prediction in the IF stage rather than in the branch prediction system (see Col.2 lines 1-10 and Col.5 lines 14-20). Furthermore, if there was no instruction selected based on a branch prediction, then having branch prediction in the processor would be moot and an extraneous feature, adding unnecessary hardware and complexity to the system.

d. Updating the branch history and the stored branch prediction reference data in the branch prediction table in response to a real branch address according to an execution result of the conditional branch instruction (see Col.3 lines 35-41, 47-50). Here, because branch prediction is based on the fact that future outcomes of conditional branches will be similar to prior outcomes (see Col.2 lines 1-10), and because Talcott has taught the storing the results of prior branch instructions in the history register and the branch prediction table (see Col.3 lines 35-41, 47-50),

it is inherent that a branch instruction has been executed and the results of the execution are used to update the history register and branch prediction table.

24. Regarding claim 11, Talcott has taught the method of claim 10, further comprising the steps of:

a. Determining whether the real branch address matches with the branch prediction address (see Col.3 lines 35-41, 47-50). Here, as shown above in paragraph 21, it is inherent that a branch instruction has been executed and the results of the execution are used to update the history register and branch prediction table. Furthermore, it is inherent in the updating of the history register and branch prediction table that there must be a comparison between what was predicted and the actual result of the branch instruction being executed so that the register and table can be updated to contain accurate information so that branches can be predicted accurately and in an educated manner (see Col.2 lines 1-10).

b. Changing and outputting the corrected branch address to the branch address if the real branch address does not match therewith (see Col.3 lines 44-50, Col.3 line 60 to Col.4 line 7). Here, when the control signal is "0", a branch has been predicted incorrectly (see above paragraph 17). Therefore it is inherent that the real, correct branch address be selected and subsequently output to the instruction fetch circuitry (290 of Fig.2) so that the microprocessor operates correctly.

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

26. Kulkarni et al., U.S. Patent No. 5,742,805, has taught a branch prediction method using a history register whose output is used in a hashing function to index a branch prediction table, whose output is used to make an educated branch prediction.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 7am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
12/17/2003

RICHARD L. ELLIS
PRIMARY EXAMINER